REMARKS

Claims 1-37 are pending. Claims 1, 11, 21, 24, 27, and 30 are independent claims. Claims 1, 11, 24, 27, and 30 are amended in this response. No new matter is added. Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1, 2, 4, 5, 11, 12, 14, 15, 21, 22, 24, 25, 27, 28, 30, 31, and 33-37 stand rejected under 35 USC 103(a) as allegedly being obvious over Pereira et al. (US 6,697,276), hereinafter "Pereira," in view of Wolrich et al. (US Patent Application Publication No. 2003/0115347), hereinafter "Wolrich," with "Howstuffworks 'What is a packet?' by Marshall Brain", hereinafter "Howstuffworks," offered as extrinsic evidence. Claims 3, 6-10, 13, 16-20, 23, 26, 29, and 32 stand rejected under 35 USC 103(a) as allegedly being obvious over Pereira in view of Wolrich and further in view of Litt et al (US Patent Application Publication No. 2003/0126358), hereinafter "Litt." The rejections are respectfully traversed. The references, Pereira, Wolrich, and Litt, taken alone, or in any combination, do not describe or suggest the features of the claimed subject matter.

As amended, claim 1 recites, "allocating a memory entry in a memory device to executable instructions to be executed on a multithreaded engine included in a packet processor; and including a unique identifier assigned to the executable instructions in a portion of the memory entry." (Emphasis added). Pereira does not describe or suggest all the features of claim 1.

Pereira describes a content addressable memory (CAM) device having a memory, a hash index generator to associate a search value with a unique location within a memory, and a compare

circuit. See, e.g., Pereira at Abstract. Pereira does not describe or suggest, "including a unique identifier assigned to the executable instructions in a portion of the memory entry," as recited in claim 1. The cited portion of Pereira states:

> The entry type value programmed within the configuration register of each hash CAM block also allocates the hash CAM block to a logical group of one or more hash CAM blocks referred to herein as an entry type pool. In one embodiment, each hash CAM block is allocated to one of a finite number of entry type pools which are used to store only entries having the programmed entry type. For example, a first set of hash CAM blocks may be allocated (i.e., by appropriate assignment of entry type values within their respective configuration registers) to an IPv4 pool, a second set of hash CAM blocks may be allocated to an MPLS pool, a third set of hash CAM blocks may be allocated to a packet classification pool, a fourth set of hash CAM blocks may be allocated to an IPv6 pool, and so forth. (Emphasis added).

See, Pereira, col. 18, lines 36-49 .

Thus, as described in Pereira, the hash CAM block is allocated to a logical group of one or more hash CAM blocks, e.g., by appropriate assignment of entry type values within their respective configuration registers. Pereira does not describe or suggest that the logical group, to which the hash CAM block is allocated, is included in the hash CAM block. In contrast, claim 1 describes including a unique identifier assigned to the executable instructions in a portion of the memory entry allocated to the executable instructions. Thus, Pereira does not describe or suggest this feature of the claimed subject matter.

The Office Action acknowledges that Pereira does not describe or suggest a multithreaded engine as claimed and relies on Wolrich solely for Wolrich's teaching of a multithreaded engine. Further, Litt does not describe or suggest "including a

unique identifier assigned to the executable instructions in a portion of the memory entry," as claimed. Therefore, neither Pereira nor Wolrich nor Litt, taken alone or in any combination describe or suggest all the features recited in claim 1. Accordingly, a *prima facie* case of obviousness is not established.

Further, it is respectfully submitted that the reliance on Wolrich is inappropriate because the Office Action relies on hindsight to arrive at the determination of obviousness. In this regard, the Office Action describes that the motivation for combining Pereira and Wolrich would have been to not have the processor lie idle. See, e.g., Office Action, page 4, paragraph 3. However, Wolrich already describes a method to avoid processor idling. The cited portion of Wolrich states:

> By pipelining, the programming engine can perform the first stage of execution of an instruction and when the instruction passes to the next stage, a new instruction can be started. The processor does not have to lie idle while waiting for all steps of the first instruction to be completed. Therefore, pipelining can lead to improvements in system performance.

See, Wolrich, [0014].

Thus, Wolrich describes a method for improving system performance where the processor does not have to lie idle. The advantage, that the Office Action contends would be achieved by the suggested combination of Pereira and Wolrich, is already achieved by Wolrich. Therefore, it is respectfully submitted that one skilled in the art would not be motivated to combine Pereira with Wolrich to realize an advantage that is achieved by Wolrich alone.

Further, neither does Pereira describe pipelining nor does Pereira describe that the CAM device assists in pipelining. It

is respectfully submitted that the Office Action appears to rely on Applicant's disclosure to find motivation to piece together the teachings of Pereira's CAM device and Wolrich's multithreaded engine, and that such reliance is impermissible.

It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. (See *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985).) This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (See *In re Fritsch*, 23 U.S.P.Q. 2d 1780, 1784 (Fed. Cir. 1992), quoting *In re Fine*, 837 F.2d at 1075, 5 USPQ2d at 1600). Thus, the proferred motivation to combine amounts to a hindsight reconstruction using the Applicant's own disclosure as a template.

Thus, claim 1 is patentable. Claims 2-10 and 33 are also patentable at least for reasons similar to claim 1 and for the additional recitations that they contain.

Claims 11, 21, 24, 27 and 30 are also patentable at least for reasons similar to claim 1. Claims 12-20, 22, 23, 25, 26, 28, 29, 31, 32, and 34-37 are also patentable at least for similar reasons and for the additional recitations that they contain.

CONCLUSION

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition,

because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please apply any credits or charges to deposit account 06-1050.

Respectfully submitted,

Date: 8/8/01

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